REMARKS

The Office Action dated March 1, 2004 has been received and carefully noted. The above amendments to the claims and the following remarks are submitted as a full and complete response thereto.

Claim 17 has been amended to place the subject matter in clear condition for allowance. No new matter has been added, and no new issues are raised which require further consideration and/or search. Claims 11-12 and 18-31 have been allowed. Claims 1, 3-10 and 13-17 are submitted for consideration.

As a preliminary matter, the Office Action indicated that claim 17 contained allowable subject matter, and would be allowable if amended to be in independent form. Claim 17 has been amended to place the subject matter of this claim in condition for allowance.

Applicant wishes to thank the Examiner for indicating the allowance of claims 11-12 and 18-31.

Claims 1, 3-10 and 13-16 were rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,393,548 to Kerstein et al. in view of U.S. Patent No. 5,909,564 to Alexander et al. The rejection is traversed as being based on references that neither teach nor suggest the novel combination of features clearly recited in independent claims 1 and 13. Claim 1, upon which claims 3-10 depend, recites a network switch which includes a data port, a statistics counter, a statistics gathering circuit and direct memory access circuitry. The data port is used for communicating with a data network.

The statistics counter is connected to the data port for monitoring operational parameters associated with the data port. The statistics counter includes statistics registers. The statistics gathering circuit is connected to the statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory. The direct memory access circuitry wherein the statistics gathering circuit transmits the data from the statistics registers to the remote system memory via a Direct Memory Access (DMA) operation.

Claim 13, upon which claims 14-16 depend, recites a method of monitoring port activity in a network switch. The method includes the steps of storing port activity data in a statistics register on the network switch and reading the port activity data with a statistics gathering unit. The method also includes the steps of transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory; and accessing the remote system memory with a remote CPU to read the reconstructed statistics register.

As will be discussed below, the cited prior art references of Kerstein et al. and Alexander et al. fail to disclose or suggest the elements of any of the presently pending claims.

Kerstein et al. discloses a network which includes a series of switched transceivers that perform time division multiplexing and time division demultiplexing for data packets transmitted between a multiport switch and 10 Mb/s stations. Col. 4, lines 1-5. The multiple port switch includes a decision making engine, a switching engine, a buffer

memory interface, configuration registers, management counters and a MAC protocol interface to support the routing of data packets between the Ethernet ports serving network stations. Col. 4, lines 19-24. The switch includes enhanced functionality to make intelligent switching decisions, to provide statistical network information in the form of management information base objects to an external management entity and interfaces to enable external storage of packet data and switching logic in order to minimize the chip size of the switch. Col. 4, lines 24-32. The switch also includes a management port that enables the external management entity to control overall operations of the switch by a management interface. Col. 4, lines 38-41. The switch further includes a PCI interface connected to a host processor to enable the host process to access the internal IMS registers and the external memory. Col. 4, lines 41-46.

Alexander et al. discloses an Ethernet frame switch which has an Ethernet switch processor coupled to a multi-channel direct memory access (DMA) controller, medium access control (MAC) interface logic blocks, an external memory controller and an expansion bus interface logic block. Col. 2, line 64-Col 3, line 2. Ethernet frame data is accepted from terminals by the MAC interface logic blocks and buffered in the associated FIFO. The DMA controller transfers the data to external memory and notifies the Ethernet switch processor of the presence of a received frame. Col. 3, lines 9-13. After the processor inspects the frame, if the target of the frame is determined to be an end-system associated with some other MAC interface port, the Ethernet switch processor

causes the DMA controller to transfer the frame data out of the external memory to the MAC interface port. Col. 3, lines 14-23.

Applicant respectfully submits that the cited references fail to disclose all of the elements of independent claims 1 and 13. Claim 1 in part recites a statistics counter connected to said data port for monitoring operational parameters associated with the data port, said statistics counter including statistics registers therein; a statistics gathering circuit connected to said statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory; and direct memory access circuitry, wherein the statistics gathering circuit transmits the data from the statistics registers to the remote system memory via a Direct Memory Access operation. Claim 13 in part recites storing port activity data in a statistics register on the network switch; reading the port activity data with a statistics gathering unit; transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory; and accessing the remote system memory with a remote CPU to read the reconstructed statistics register.

Although the Office Action states that Kerstein et al. discloses a plurality of statistic counters for monitoring operational parameters; a statistics gathering circuit for reading the statistic register and for transmitting data from the statistic register to a remote system memory, Applicant respectfully submits that the cited portions of Kerstein et al. only discloses that the multiport switch of includes enhanced functionality to provide statistical network information in the form of management information based

objects to an external management entity. Kerstein et al. does not specify how the statistical network information is obtained. In fact, Kerstein et al. does not disclose or even suggest a statistics counter, with statistic registers, for monitoring operational parameters associated with a data port as recited in claim 1. Kerstein et al also does not disclose or suggest a statistics gathering circuit connected to the statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory; and direct memory access circuitry, wherein the statistics gathering circuit transmits the data from the statistics registers to the remote system memory via a Direct Memory Access operation as recited in claim 1. Furthermore, Kerstein et al. does not disclose or suggest reading the port activity data with a statistics gathering unit; transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory; and accessing the remote system memory with a remote CPU to read the reconstructed statistics register as recited in claim 13.

Applicant respectfully submits that Alexander et al. fails to cure the deficiencies of Kerstein et al. According to Alexander et al, the DMA controller transfers the data to external memory and notifies the Ethernet switch processor of the presence of a received frame. Col. 3, lines 9-13. Alexander et al. further discloses that after the processor inspects the frame, if the target of the frame is determined to be an end-system associated with some other MAC interface port, the Ethernet switch processor causes the DMA controller to transfer the frame data out of the external memory to the MAC interface

port. Col. 3, lines 14-23. Applicant submits that Alexander et al. in no way discusses or even suggests a statistics counter, with statistics registers, for monitoring operational parameters associated with the data port as recited in claim 1. Alexander et al. also fails to disclose or suggest a statistics gathering circuit connected to the statistics counter for reading the statistics registers, and for directly transmitting data from the statistics registers to a remote system memory; and direct memory access circuitry, wherein the statistics gathering circuit transmits the data from the statistics registers to the remote system memory via a Direct Memory Access operation as recited in claim 1. Alexander et al. also does not disclose or suggest reading the port activity data with a statistics gathering unit; transmitting the port activity data directly to a remote system memory, thereby reconstructing the statistics register in the remote system memory; and accessing the remote system memory with a remote CPU to read the reconstructed statistics register as recited in claim 13. Therefore, Applicant respectfully asserts that the rejection under 35 U.S.C. §103(a) should be withdrawn because neither Kerstein et al. nor Alexander et al. whether taken singly or combined, teaches or suggests each feature of claims 1 and 13 and hence, dependent claim 3-10 and 14-16 thereon.

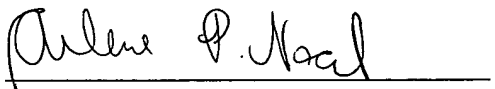
As previously noted, claim 17 was indicated as containing allowable subject matter and claim 17 has been amended to place that claim in clear condition for allowance. It is further noted that each of claims 1, 3-10 and 13-16 recited subject which is neither disclosed nor suggested in the cited prior art reference. It is therefore

respectfully requested that all of claims 1, 3-10 and 13-17 be allowed, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



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